

<b>Notice of References Cited</b>	Application/Control No. 10/017,777		Applicant(s)/Patent Under Reexamination KUZEMCHAK ET AL.	
	Examiner Ted T. Vo		Art Unit 2122	Page 1 of 1

**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,949,993	09-1999	Fritz, David Carroll	703/22
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Guerra et al., "Cycle and Phase Accurate DSP Modeling and Integration for HW/SW Co-Verification", ACM, pages: 964-969, June 1999.
	V	Levitt et al., "A Scalable Formal Verification Methodology for Pipelined Microprocessors", ACM, pages 1-6, 1996.
	W	
	X	

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.